# MIHICTEPCTBO ОСВITИ I НАУКИ УКРАЇНИ <br> Національний університет «Запорізька політехніка» 

## МЕТОДИЧНІ ВКАЗІВКИ

до виконання лабораторних робіт з дисципліни
«Основи електроніки та мікросхемотехніки»
для студентів спеціальності 141 - Електроенергетика, електротехніка
та електромеханіка всіх форм навчання
з англійською мовою навчання

Методичні вказівки до виконання лабораторних робіт 3 дисципліни «Основи електроніки та мікросхемотехніки» для студентів спеціальності 141 - Електроенергетика, електротехніка та електромеханіка всіх форм навчання» з англійською мовою навчання. /Укл.: М.О. Поляков - Запоріжжя: НУ «Запорізька політехніка», 2024. -52 c.

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## INTRODUCTION

The purpose of the laboratory work is to consolidate the theoretical material from the discipline "Fundamentals of Electronics and Microcircuits" in practice. For the study of electronic devices, nodes and units can be used any circuit design software: the Electronics Workbench (EWB), Multisim, Tinkercad or Sircuit Simulate.

The advantage of computer simulation is the large variety of electronic elements and measurement tools to create an electronic circuit, the impossibility of its damage and a high level of electrical safety.

The guidelines provide a description of 13 laboratory works on the topics of the study of the user interface of Electronics Workbench, semiconductor diodes, bipolar transistors, thyristors, electronic amplifiers, operational amplifiers, logic elements, filters, combinational units, triggers, counters, voltage regulates, DACs and ADCs, pulse power regulators.

The student is obliged to study the theoretical material, perform practical tasks, make a report on laboratory work, which will have the main sections:

1. Name of laboratory work.
2. Its purpose.
3. Schemes of experiments, tables, graphs, calculations, conclusions.

The report must be prepared in accordance with DSTU 3008-2015 and protected.

## Laboratory work № 1 The simulate program

Objective: to learn the interface of the simulate program, get skills of construction of electric circuits and use of oscillograph.

Short theoretical data: Software products for circuit modeling allow you to synthesize electrical components from individual elements, observe changes in currents and voltages in the branches and nodes of the circuit, change the parameters of component models, and perform circuit analysis. A special feature of these packages is the presence of control and measuring instruments, which in appearance, controls and descriptions are as close as possible to their industrial analogues, which makes it possible to gain practical skills in the process of working with the most common
instruments: multimeter, oscilloscope, generators, etc. Programs are easy to learn and easy to use.

Basic techniques for working with a circuit modeling package that are used when performing subsequent laboratory work:

- Find the required element and place it in the work field.
- Change the orientation and model parameters of an element.
- Connect elements together.
- Run the assembled circuit and observe the results using measuring instruments.


## Motion of work

## Experiment №1

1. To lay down the chart of the resistive voltage divider, represented on fig. 1.1.


Figure 1.1-Scheme of resistive voltage divider
2. Determine the current flowing through the resistor R1 and the voltage on the resistor R2, add them to the table. 1.1. Take off the instrumentation for several voltage values of the power supply E1. Construct a graph of current dependence on voltage.

Table 1.1 - Devices show

| $\mathrm{I}, \mathrm{mA}$ |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{U}, \mathrm{V}$ |  |  |  |  |  |  |  |  |

Experiment №2
3 Make a circuit of a single-phase bridge rectifier, working on an active load, depicted in Fig. 1.2.


Figure 1.2 - Scheme of single-phase bridge rectifier, working on active load

4 Set up the oscilloscope and take an oscillogram.

## Control questions

1. Features and tasks of the program for modeling electrical circuits.
2. How to print a circuit diagram on a printer.
3. What command can you use to copy a diagram into a report.
4. How to change the color of the conductor and when to do it.
5. Which command can assign a positional value to a circuit component and what rule is used.
6. How can you set the parameters of the circuit components (for example, model, rating, temperature, etc.).

## Laboratory work №2 The semiconductor diode

Objective: to obtain the skills of simulation of diode circuits, to study the direct and reverse branches of the VAC diode.
Brief theoretical data: The semiconductor diode is an electronic device with a nonlinear voltage-current characteristic (VAC). Using a simulation program, it is easy to simulate and measure the diode voltage and diode
current by connecting it to a voltage source of various ratings through a resistor. Depending on the polarity of the diode, each result of measuring current and voltage corresponds to a point on the forward or reverse branch of the diode's current-voltage characteristic. The measurement results are affected by the resistance of the measured devices. Therefore, the schemes for measuring the forward and reverse branches of the current-voltage characteristic are somewhat different.

## Motion of work

Experiment №1
1 Draw a diagram depicted in Fig. 2.1.


Figure 2.1 - Diagram of research of direct branch of VAC diode
2 When changing the voltage E1 or resistance R1, take measurements of the measuring devices and add them to the tabl. 2.1.

3 According to tabl. 2.1, to construct a graph of the straight line of the VAC.

4 According to tabl. 2.1, calculate the resistance of the Rd diode by direct current and construct a dependency curve resistance based on the voltage on the diode.

Table 2.1 - Impressions of Measured Devices

| $\mathrm{U} 1, \mathrm{~V}$ |  |  |  |  |  |  |  |
| :---: | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{I} 1, \mathrm{~mA}$ |  |  |  |  |  |  |  |
| $\mathrm{R}_{\mathrm{d}}, \Omega$ |  |  |  |  |  |  |  |

## Experiment №2

5. According to the variant number, choose a diode from the tabl.2.2.
6. Collect the diagram shown in fig. 2.2.

Table 2.2 - Options for diodes

|  | - | $\sim$ | m | $\checkmark$ | in | $\bigcirc$ | $\checkmark$ | $\infty$ | $a$ | $\bigcirc$ | $=$ | $\simeq$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\frac{\square}{0}$ | $\begin{aligned} & \infty \\ & \underset{Z}{\underset{Z}{z}} \end{aligned}$ | $\underset{\underset{Z}{\underset{Z}{Z}}}{\substack{\text { an }}}$ | $\begin{aligned} & \text { B } \\ & \frac{n}{7} \end{aligned}$ | $\begin{aligned} & \bar{n} \\ & \stackrel{7}{2} \end{aligned}$ | $\frac{\sqrt{n}}{\frac{7}{2}}$ | $\begin{gathered} n \\ \frac{\pi}{7} \end{gathered}$ | $\begin{aligned} & \underset{2}{U} \\ & \underset{Z}{7} \end{aligned}$ | $\begin{aligned} & \text { n } \\ & \stackrel{y}{Z} \\ & \underset{Z}{2} \end{aligned}$ | $$ |  |  | $\stackrel{G}{\underset{Z}{Z}}$ |



Figure 2.2 - Scheme of the study of the reverse branch of the VAC diode
7. By changing the voltage E1, get the VAC points and add them to the tabl. 2.3.

Table 2.3 - Impressions of Measured Devices

| E1, V |  |  |  |  |
| :---: | :--- | :--- | :--- | :--- |
| I1, mA |  |  |  |  |
| U1, V |  |  |  |  |


| $\mathrm{R}, \mathrm{k} \Omega$ |  |  |  |
| :--- | :--- | :--- | :--- | :--- |

8. Determine the breakdown voltage.
9. Write the diode parameters in the report.

## Control questions

1. How to determine the current through the diode.
2. Why are different circuits used to study the direct and reverse side of VAC.
3. How to determine the resistance of the diode for DC , differential resistance.
4. When is the extraction and injection of current carriers in the diode.
5.Ividence of the breakdown of the diode: definition, mechanisms, area on the VAC.

6 . What is the real diode from the ideal.

## Laboratory work №3 The bipolar transistor

Objective: to investigate the VAC of a bipolar transistor in a common emitter scheme.

Brief theoretical data: The bipolar transistor is a semiconductor device used to amplify current and (or) voltage in electronic amplifiers. The family of output characteristics of the transistor according to the scheme with the common emitter (CE) is described by the dependence $I_{C}=f\left(U_{C E}\right)$ with $I_{B}=$ const. In turn, the family of input characteristics of the transistor by the scheme of CE is described by the dependence $I_{B}=f\left(U_{B E}\right)$ with $U_{C E}=$ const.

Static current transfer coefficient of the base is defined as the ratio of collector current $I_{C}$ to base current $I_{B}$ :

$$
\beta_{D C}=\frac{I_{C}}{I_{B}}
$$

The differential coefficient of current transfer of the base $\beta_{\mathrm{AC}}$ The differential transfer coefficient of the base current is determined from the output characteristic of the transistor as the ratio of the current increase $\Delta$ Ic
of the collector current to the increase $\Delta \mathrm{I}_{\mathrm{b}}$ of the base current that causes it at a fixed value of the collector-emitter voltage.

$$
\beta_{A C}=\frac{\Delta I_{C}}{\Delta I_{B}}
$$

Differential input resistance of $\mathrm{r}_{\text {IN }}$ transistor in the circuit with CE is determined by the input VACs at a fixed value of the collector-emitter voltage. It can be found as the ratio of the voltage change $\Delta U_{B E}$ to the baseemitter to the change caused by it $\Delta \mathrm{I}_{\mathrm{B}}$ base current:

$$
r_{I N}=\frac{\Delta U_{B E}}{\Delta I_{B}} .
$$

Similarly, in the output VAC, the output impedance of the transistor $r_{\text {OUT }}$ in the circuit with the total emitter is determined:

$$
r_{O U T}=\frac{\Delta U_{C E}}{\Delta I_{C}} .
$$

## Motion of work

Experiment №1
1 Draw a pattern of fig. 3.1. Transistor for the circuit to choose according to the number of the variant from the tabl. 3.1.

Table 3.1 - Options for transistors for the circuit

| Variant | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\begin{aligned} & \stackrel{\rightharpoonup}{n} \\ & \hat{O} \\ & \underset{\sim}{0} \end{aligned}$ | $\begin{aligned} & \text { Oि } \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & \stackrel{\rightharpoonup}{\Omega} \\ & \text { O} \\ & \text { Un } \end{aligned}$ | $\begin{aligned} & \text { M } \\ & \underset{\sim}{\infty} \\ & \stackrel{\sim}{\sim} \end{aligned}$ | $\begin{aligned} & \stackrel{\sim}{\sim} \\ & \underset{\sim}{\infty} \\ & \underset{\sim}{u} \end{aligned}$ | $\begin{aligned} & \stackrel{\sim}{q} \\ & \underset{\sim}{\infty} \\ & \underset{\sim}{\#} \end{aligned}$ | $\begin{aligned} & \text { N్ల } \\ & \text { N} \\ & \text { 弋̃ల } \end{aligned}$ | $\begin{aligned} & \text { Oै } \\ & \underset{\sim}{\infty} \\ & \underset{\sim}{0} \end{aligned}$ | $\begin{aligned} & \text { ले} \\ & \text { N } \\ & \text { స్ల } \end{aligned}$ | $\begin{aligned} & \stackrel{\sim}{m} \\ & \underset{\sim}{\sim} \\ & \underset{\sim}{u} \end{aligned}$ | $\underset{\sim}{\underset{\sim}{\sim}}$ | O 0 0 0 0 |



Figure 3.1 - Scheme for the research of a transistor VAC with a common emitter
2. Measure IC and $U_{C E}$ by setting $I_{B}$ as shown in tabl. 3.2.

3 Build a timetable for a family of output characteristics. According to the graph, determine the gain of the transistor and the output impedance.

4 Write in the report the parameters of the transistor model from the properties window of the component.

Table 3.2 - Experiment results

| $\mathrm{I}_{\mathrm{B}}=0 \mathrm{~mA}$ | $\begin{gathered} \mathrm{I}_{\mathrm{C}} \\ \mathrm{~mA} \end{gathered}$ |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\underset{\mathrm{VE}}{\mathrm{U}_{\mathrm{CE}}}$ |  |  |  |  |  |  |  |  |  |  |
| $\begin{gathered} \mathrm{I}_{\mathrm{B}}=0,0005 \\ \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \mathrm{I}_{\mathrm{C}} \\ \mathrm{~mA} \end{gathered}$ |  |  |  |  |  |  |  |  |  |  |
|  | $\begin{gathered} \mathrm{U}_{\mathrm{CE}}, \\ \mathrm{~V}, \end{gathered}$ |  |  |  |  |  |  |  |  |  |  |
| $\begin{gathered} \mathrm{I}_{\mathrm{B}}=0,001 \\ \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \mathrm{I}_{\mathrm{C}} \\ \mathrm{~mA} \end{gathered}$ |  |  |  |  |  |  |  |  |  |  |
|  | $\begin{gathered} \mathrm{U}_{\mathrm{CE}}, \\ \mathrm{~V}, \end{gathered}$ |  |  |  |  |  |  |  |  |  |  |
| $\begin{gathered} \mathrm{I}_{\mathrm{B}}=0,002 \\ \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \mathrm{I}_{\mathrm{C}} \\ \mathrm{~mA} \end{gathered}$ |  |  |  |  |  |  |  |  |  |  |
|  | $\mathrm{U}_{\mathrm{CE}},$ |  |  |  |  |  |  |  |  |  |  |

Experiment №2
5.Set the $\mathrm{U}_{\mathrm{CE}}$ voltage to $(0 ; 10)$ volt by changing the $\mathrm{E}_{\mathrm{C}}$.

6 When changing $\mathrm{E}_{\mathrm{C}}$, get the voltage $\mathrm{U}_{\mathrm{BE}}$ in the range from 0 to 0.75 volts (at least 10 values). For each $\mathrm{U}_{\mathrm{BE}}$ to record $\mathrm{I}_{\mathrm{B}}$, the results are recorded in the tabl. 3.3.

7 Construct a graph of input characteristics $\mathrm{I}_{\mathrm{B}}=\mathrm{f}\left(\mathrm{U}_{\mathrm{BE}}\right)$, at $\mathrm{U}_{\mathrm{CE}}=$ const. According to the graph, determine the input impedance of the transistor.

Table 3.3 - Experiment results

| $\begin{gathered} \mathrm{U}_{\mathrm{CE}}= \\ 0, \mathrm{~V} \end{gathered}$ | $\mathrm{E}_{\mathrm{C}}, \mathrm{V}$ |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\mathrm{U}_{\mathrm{BE}}, \mathrm{V}$ |  |  |  |  |  |  |  |  |  |
|  | $\mathrm{I}_{\mathrm{B}}, \mathrm{mA}$ |  |  |  |  |  |  |  |  |  |
| $\begin{aligned} & \mathrm{U}_{\mathrm{CE}}= \\ & 10, \mathrm{~V} \end{aligned}$ | $\mathrm{E}_{\mathrm{C}}, \mathrm{V}$ |  |  |  |  |  |  |  |  |  |
|  | $\mathrm{U}_{\mathrm{BE}}, \mathrm{V}$ |  |  |  |  |  |  |  |  |  |
|  | $\mathrm{I}_{\mathrm{B}}, \mathrm{mA}$ |  |  |  |  |  |  |  |  |  |

## Control questions

1. Principle of operation, varieties, operating modes, switching circuits, characteristics and models of the bipolar transistor.
2. What does the collector current of the transistor depend on?
3. What expression describes the output characteristic of the transistor, and under what condition is it valid?
4. What is the expression describing the input characteristic of the transistor, and under what condition is it valid?
5. Does the $\beta_{\mathrm{DC}}$ coefficient depend on the collector current? If so, then which degree?
6. What can be said on the initial characteristics of the dependence of collector current on the current of the base and the voltage collectoremitter?
7. What parameters of the transistor can be determined by its input and output VAC?

Laboratory work №4. The transistor amplifier
Objective: Explore a transistor amplifier.

Brief theoretical data: in this paper, the principle of calculating a one-stage amplifier with CE is investigated. When calculating the cascade transistor is replaced by its simplified equivalent circuit. Cascade calculation is performed in two stages. The calculation of constant components allows you to find the parameters of the working point of the transistor cascade. Calculation of the variable components is the enhancement of the cascade properties at this point.

By using an equivalent circuit, the constant components of the current of the base of the $\mathrm{I}_{\mathrm{BP}}$, the current of the $\mathrm{I}_{\mathrm{CP}}$ collector and the voltage on the $U_{C P}$ collector are found. They are defined by the following expressions:

$$
\begin{aligned}
& I_{B P}=\frac{E_{E C V}-U_{B E 0}}{R_{B}} \\
& I_{C P}=\beta \cdot I_{B P} \\
& U_{C P}=E_{C}-I_{C P} \cdot R_{C}
\end{aligned}
$$

An alternating current circuit allows you to determine the amplitudes of the alternating current components of the base $\mathrm{I}_{\mathrm{B}-\mathrm{M}}$, the collector current $\mathrm{I}_{\mathrm{C}-\mathrm{M}}$, the voltage on the collector. With a known value of the amplitude of the voltage of the generator EGM, the amplitude of currents and voltages can be determined by the following expressions (the sign M denotes the amplitude of the variable):

$$
\begin{gathered}
I_{B-M}=\frac{E_{G M}}{R_{I N}} \\
I_{C-M}=\beta \cdot I_{B-M} \\
U_{C-M}=I_{C-M} \cdot R_{E C V}
\end{gathered}
$$

The obtained expressions allow to determine the voltage gain $(\mathrm{K})$ as the ratio of the amplitude of the output voltage to the input:

$$
K=\frac{U_{B-M}}{E_{G M}}=\beta \cdot \frac{R_{E C V}}{R_{I N}}
$$

Instantaneous values of currents and voltages are the sum of constant and variable components. The corresponding oscillograms are shown in fig. 4.1.

The oscillograms of the alternating current components of the base $I_{B}$ and the current collector $\mathrm{I}_{\mathrm{C}}$ have the same shape, because the corresponding instantaneous values are proportional:

$$
I_{C}=\beta \cdot I_{B}
$$

The maximum value of collector current can not exceed the saturation current value:

$$
I_{C M}=E_{C} / R_{C}
$$

This current corresponds to the saturation current of the base:

$$
I_{B N}=\frac{I_{C N}}{\beta}=\frac{E_{C}}{\beta \cdot R_{C}}
$$

The instantaneous value of the voltage on the collector is determined by the expression:

$$
U_{C}=E_{C}-I_{C} \cdot R_{C}
$$

Oscillograms shown in fig. 4.1, received for mode $U_{C P}=E_{C} / 2$. In this case, you can obtain the maximum value of the undistorted output voltage, the maximum value of which amplitude is equal to half the voltage of the power supply $\mathrm{E}_{\mathrm{C}}$.

The considered oscillograms (Fig 4.1) correspond to the linear mode of the amplifier's operation.

Experiment №1
Specifying a work point

1. Gather the scheme shown in fig. 4.2. In the scheme use the transistor, selected from the tabl. 4.1 according to the option.
2. When changing R1 to get Ups (attention, switches S1, S2 must be in the position shown in fig. 4.2, S 1 is open, and S 2 is locked).
3. Calculate collector current for a resting point


Figure 4.1 －Oscilloscope of the amplifier in linear mode Motion of work

Table 4．1－Models of transistors and data for experiment number 1

|  | － | $\sim$ | m | $\checkmark$ | in | $\bigcirc$ | $\wedge$ | $\infty$ | $\bigcirc$ | $\bigcirc$ | $=$ | $\sim$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{aligned} & \text { O} \\ & \text { O } \\ & \stackrel{O}{O} \\ & 0 \end{aligned}$ |  | $\begin{aligned} & \sim \sim \\ & \sim \\ & \underset{\sim}{\infty} \\ & \text { Un } \end{aligned}$ | $\begin{aligned} & \text { O} \\ & \underset{\sim}{\infty} \\ & \underset{\sim}{\infty} \end{aligned}$ | $\begin{aligned} & \tilde{\sim} \\ & \stackrel{\sim}{\infty} \\ & \underset{\sim}{\infty} \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \text { ~} \\ & \underset{\sim}{\infty} \\ & \underset{\sim}{\tilde{0}} \end{aligned}$ | $\begin{aligned} & \text { M} \\ & \text { N} \\ & \text { ָ̈n } \end{aligned}$ | $\begin{aligned} & \stackrel{\sim}{m} \\ & \underset{\sim}{7} \\ & \underset{\sim}{J} \end{aligned}$ |  | $\begin{aligned} & \text { en } \\ & 0 \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ |
| ベص | 은 | $=$ | $\simeq$ | $\cdots$ | $\pm$ | $\bigcirc$ | $\wedge$ | $\stackrel{\infty}{\sim}$ | $\bigcirc$ | $\stackrel{\sim}{2}$ | $\bar{\sim}$ | ה |
| 号ص． | in | n | $\bigcirc$ | $\bigcirc$ | $\checkmark$ | $\infty$ | $\infty$ | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ | ＝ | $=$ |



Figure 4.2 - Transistor amplifier circuit
Experiment №2
Investigation of the amplifier in low signal mode
4. Specify source options E according to the option. The parameters are presented in the tabl. 4.2.
5. Connect the oscilloscope to the source of the input signal and to the transistor collector. Connect the source of the input signal to the transistor base using the S1 switch.
6. Remove the oscillogram, determine the maximum and minimum voltages on the collector on it and the voltage gain of the cascade. Determine the maximum voltage of the source of the input signal, in which the output signal has an undamaged form.

Table 4.2 - Parameters of the voltage source

|  | - | $\sim$ | m | $\checkmark$ | in | $\bigcirc$ | $\checkmark$ | $\infty$ | $a$ | $\bigcirc$ | च | $\sim$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ェิص | in | $\bigcirc$ | $\checkmark$ | $\infty$ | $\bigcirc$ | $\bigcirc$ | in | $\bigcirc$ | $\wedge$ | $\infty$ | $\bigcirc$ | $\bigcirc$ |
| $\rightarrow \sim$ N | 8 | 윽 | $\stackrel{\sim}{n}$ | ৪ | \& | $\stackrel{i}{f}$ | $8$ | $8$ | $\infty$ | ¢ | 8 | 8 |

## Control questions

1. Definition, classification, structural diagram, characteristics and parameters of the electronic amplifier.
2. Varieties and elements of the amplifier stages.
3. Point of rest of the amplifier cascade: definition, methods of the task.
4. What is the difference between the phases between the input and output sinusoidal signals in the amplifier with CE and CC.
5. How does the input impedance affect the voltage gain.
6. Variety of distortions of the output signals of the amplifier.
7. Is the output impedance of the amplifier with a high value.
8. What is the main advantage of the amplifier circuitry with CC?

## Laboratory work № 5. The operational amplifier

Objective: to investigate typical nodes on operational amplifiers inverting, non-inverting, summing, differentiating, and integrating amplifiers.

Brief theoretical data: an operating amplifier is called a highquality integrated DC amplifier with differential input and one-step output. Opamps are used to amplify, limit, summate, filter, generate, stabilize signals in analog devices.

The gain of the circuit of the non-inverting amplifier on the opamp (fig. 5.1) is determined by the formula:

$$
K s=1+R 1 / R 2
$$



Figure 5.1 - Scheme of non-inverting amplifier
The gain of the circuit of the inverting amplifier on the Opamp (fig. 5.2 ) is determined by the formula:

$$
\mathrm{Rs}=-\mathrm{R} 2 / \mathrm{R} 1 .
$$

The minus sign in the formula will indicate that the output voltage of the inverting amplifier is in the opposite phase with the input voltage


Figure 5.2 - Scheme of inverting amplifier

In the summing amplifier fig. 5.3, if the input currents and bias voltages are equal to zero, then the following ratios are performed:

$$
\begin{gathered}
\mathrm{I} 1=\mathrm{U} 1 / \mathrm{R} 1 ; \\
\mathrm{I} 2=\mathrm{U} 2 / \mathrm{R} 2, \mathrm{I}=\mathrm{I} 1+\mathrm{I} 2 \\
\mathrm{Ioc}=\mathrm{I} 1+\mathrm{I} 2=-\mathrm{U}_{\mathrm{OUT}} / \mathrm{Roc.}
\end{gathered}
$$

From these relations we obtain an expression for the output voltage:

$$
\mathrm{U}_{\text {OUT }}=-(\mathrm{I} 1+\mathrm{I} 2) * \mathrm{Roc}=-(\mathrm{U} 1 / \mathrm{R} 1+\mathrm{U} 2 / \mathrm{R} 2) * \mathrm{Roc} .
$$

If $\mathrm{Roc}=\mathrm{R} 1=\mathrm{R} 2$, then $\mathrm{U}_{\mathrm{OUT}}=\mathrm{U} 1+\mathrm{U} 2$.


Figure 5.3 - Schematic of adding amplifier
On the basis of OP can be built integrators. Figure 4.5 shows a scheme that performs this function. The following relationships are valid for this scheme:

$$
\begin{gathered}
\mathrm{U}_{\mathrm{IN}} / \mathrm{R}=-\mathrm{C}^{*} \mathrm{dU}_{\mathrm{OUT}} / \mathrm{dt}, \\
\mathrm{U}_{\mathrm{OUT}}=-1 / \mathrm{RC} * \int_{0}^{t} \mathrm{U}_{\mathrm{IN}}^{*} * \mathrm{dt}+\mathrm{const}
\end{gathered}
$$



Figure 5.4 - Integrator scheme
For the differentiator circuit (fig. 5.5), the output voltage Uout is proportional to the change in the input signal and is determined by the formula:

$$
\mathrm{U}_{\mathrm{OUT}}=-\mathrm{R} 2 * \mathrm{C} * \frac{d U_{I N}}{d t}
$$



Figure 5.5 - Differentiator scheme

## Motion of work

Experiment №1
Non-inverting amplifier
1 Draw a pattern fig. 5.1.
2 Connect the oscilloscope and pulse generator.
3 Remove the oscillogram, determine the gain and compare with the calculated.

Experiment №2
Inverting Amplifier
4 Draw a pattern of fig. 5.2.
5 Connect the oscilloscope and pulse generator.
6 Remove the oscillogram, determine the gain and compare with the calculated.

Experiment №3
Adding amplifier
7. Draw a diagram of fig. 5.3.
8. Connect the multimeter.
9. Determine the output voltage and compare it with the calculated.

Experiment №4
Integrator
10. Draw the diagram fig. 5.6.
11. Remove the oscillogram of the input and output voltage when applying voltage to the input in the form of successive rectangular pulses.


Figure 5.6 - Integrator scheme
Experiment №5
Differentiator
12. Draw a diagram of fig. 5.7.
13. Remove the oscillogram of the input and output voltage when applying voltage to the input in the form of successive rectangular pulses.


Figure 5.7 - Differentiator scheme

## Control questions

1. What is an operating amplifier.
2. What is the difference between inverting amplifier and noninverting.
3. Transfer characteristic of OPAmp for inverting and non-inverting inclusion.
4. What are the default nodes for OPAmps.
5. Write formulas for the transfer coefficient for typical nodes in OPAmps.

## Laboratory work №6. The logical elements and functions

Objective: to investigate logical elements and functions.
Brief theoretical data: variables considered in algebra of logic can accept only two values - " 0 " or " 1 ". In the algebra of logic defined: the relation of equivalence (denoted by the sign $=$ ); addition operation (disjunction), which is indicated by a sign or + ; multiplication operation (conjunction), denoted by a sign or $\&$; or a point; inversion operation denoted by an over-mark or apostrophe sign [1,2].

The algebra of logic is determined by the system of axioms:

$$
\begin{aligned}
& \left\{\begin{array}{l}
\mathrm{x}=0, \text { if } \mathrm{x} \neq 1 ; \\
\mathrm{x}=1, \text { if } \mathrm{x} \neq 0 ;
\end{array}\right.
\end{aligned}\left\{\begin{array}{l}
\overline{0}=1 ; \\
\overline{1}=0 ;
\end{array}\right]\left\{\begin{array}{l}
1 \wedge 1=1 ; \\
0 \vee 0=1 ; \\
0 \vee 1=1 \vee 0=1 ;
\end{array} \quad \begin{array}{l}
0 \wedge 0=0 ; \\
0 \wedge 1=1 \wedge 0=0
\end{array}\right] .
$$

Since the domain of definition of any function of $n$ variables is finite, such a function can be given by the table of values $f(\mathrm{Vi})$, which it takes at points Vi, where $\mathrm{i}=0,1 . .2^{(\mathrm{n}-1)}$. Such tables are called truth tables.

Logical expressions are usually executed in conjunctive or disjunctive normal forms. In a disjunctive form logical expression are written as a logical sum of logical sets, in a conjunctive form, the logical multiplication of logical sums. The procedure is the same as in ordinary algebraic expressions.

Any logical expression composed of n variables $x_{n}, x_{n-1} \ldots x_{1}$ using a finite number of operations of logic algebra can be regarded as some function of $n$ variables. Such a function is called logical.

The following features of the two variables x and y represent the main interest:
$\mathrm{f} 1(\mathrm{x}, \mathrm{y})=x \wedge y-$ logical multiplication (conjunction),
$\mathrm{f} 2(\mathrm{x}, \mathrm{y})=x \vee y-$ logical addition (disjunction),
$\mathrm{f} 3(\mathrm{x}, \mathrm{y})=\overline{x \cdot y}-$ logical multiplication with inversion
$\mathrm{f} 4(\mathrm{x}, \mathrm{y})=\overline{x \vee y}-$ logical addition with inversion
$\mathrm{f} 5(\mathrm{x}, \mathrm{y})=x \bar{y} \vee \bar{x} y-$ summing modulo " 2 ",
$\mathrm{f} 6(\mathrm{x}, \mathrm{y})=x y \vee \overline{x y}-$ equilibrium.
A physical device that implements one of the operations of logic algebra or a simpler logical function is called a logical element. A schema composed of a finite number of logical elements working on defined rules is called a logical scheme.

## Motion of work

## Experiment №1

Research Logical functions "and"
1 Follow the scheme fig 6.1.
2 Turn on the circuit, install a switch "B" at the bottom and then at the top position, then use a voltmeter on the input " B " and replace it with a logic probe for a logical signal.

3 Fare on entering the schema of the service can combo combining the logical signal "A" and "B" that for the leather combo fixing the signal "Y".

4 Record a table of logistic schema "and".


Figure 6.1 - Scheme for research logically functions "and"
Experiment №2
Investigation of logic circuits using the word generator
3. Draw a schematic diagram of Fig. 6.2.
4. Turn on the circuit.
5. Specify which terminals the chip 7400 " connects to the power supply, how many elements "2And-No" in this chip, how many elements are used in this experiment, and as the inputs and outputs used in the scheme are indicated.

6 Set the generator to step-by-step operation by pressing the "Step" button on the magnified image of the generator. Each click of the "Step" button causes a transition to the next word of a given sequence, which is fed from the output of the generator. Serializing the words of a given sequence on a chip, fill in the truth table of the element " 2 And-No".

Experiment №3
Realization of the logical function of 3 variables
Realize the function $f=a b \vee \bar{b} c$ on elements "2And-No". To do this, follow these steps:
7. Call a logic converter.
8. Enter the logical expression from the keyboard in the bottom window of the converter panel (operations "OR" correspond to the + sign, the inversion is indicated by the apostrophe).


Figure 6.2 - Ship 7400
9. Press the $A \mid B \rightarrow$ NAND key on the logic converter panel and redraw the synthesized circuit.
10. To the scheme connect the word generator (fig. 6.3), programmed to form 7 words, corresponding to numbers from 0 to $7: 0=$ $000 ; 1=001 ; 2=010 ; 3=011 ; 4=100 ; 5=101 ; 6=110 ; 7=111$.
12. Translate the word generator into step-by-step mode.
13. Turn on the scheme.
14. Serialize the specified words to the inputs of the circuit and determine the signal level at the output of the circuit with a logical probe, fill the truth table.


Figure 6.3 - Logic scheme

## Control questions

1. What is a logical variable and a logical signal? What values can they take.
2. What is a logical function and which ones do you know.
3. What is the truth table.

## Laboratory work № 7. The thyristor.

Objective: to study the principle of the thyristor and how to activate it.

Brief theoretical data: a thyristor is a semiconductor device with three or more p-n transitions used in powerful circuits. For the thyristor to be turned on, an on-line voltage is applied to its anode, which exaggerates the voltage of the thyristor. Another way to turn on the thyristor is to turn it on with a current through the thyristor control electrode. Simistor is a kind of thyristor, which can go into an activated state both in the direct and at the return voltage at the anode.

## Motion of work

Experiment №1
Investigation of thyristor when $\mathrm{U}_{\mathrm{E}}<\mathrm{U}_{\text {VDRM }}$
1 Draw a diagram of fig. 7.1.
2 The value of the amplitude of the input voltage source is set to be less than the value of the forward breakover voltage ( $\mathrm{V}_{\text {DRM }}$ ) parameter of the thyristor model.

3 Connect the oscilloscope, remove the oscilloscope.
4 Determine the operation mode of the thyristor.


Figure 7.1 - Turn on the thyristor on the anode circuit

Experiment №2
Thyristor research when $U_{E}>U_{\text {VDrM }}$
1 Repeat Experiment 1, but the value of the amplitude of the input voltage source is set to be greater than the value of the forward breakover voltage (VDRM) parameter of the thyristor model.

2 Connect the oscilloscope, remove the oscillogram.
3 Determine the operation mode of the thyristor.
Experiment №3
Turn on the thyristor in the control circuit
4. Draw a schematic diagram of fig. 7.2.
5. The value of the amplitude of the input voltage source is set to be less than the value of the forward breakover voltage (VDRM) parameter of the thyristor model.
6. Connect the oscilloscope, remove the oscillogram.
7. Determine the operation mode of the thyristor and the thyristor start delay angle.

Experiment №4
The study of the simistor
8. Draw a schematic diagram of fig. 7.3.
9. The value of the amplitude of the input voltage source is set to be less than the value of the VDRM parameter of the thyristor model.
10. Connect the oscilloscope, remove the oscillogram.
11. Determine the simistor operation mode and the timing delay of the simistor.


Figure 7.2 - Turning on the thyristor through the control circuit


Figure 7.3 - The simister research

## Control questions

1. What is called a thyristor.
2. What types of thyristors do you know.
3. Draw a diagram of the thyristor.
4. Draw and explain the VAC thyristor.
5. Differences between the thyristor of the simistor.

## Laboratory work №8. The filters

Objective: To explore passive filters electronic devices based RCand LC-circuits.

Brief theoretical data: in electronics it is often necessary to allocate a signal of a given frequency from the whole set of information and parasitic signals that enter the device's input. For this purpose, various frequency-selective schemes are used, which are called filters. The basis of any filter is the RC or LC chain, which is a passive part of the whole electronic device, that is, it is a passive filter. It is the passive filter that allocates the signals of the given frequencies from their entire spectrum, while the other part of the device performs an analog operation to amplify or generate this signal.

Common filter response specifications are described as follows:

- A low-pass filter (LPF) passes low frequencies while blocking higher frequencies (See fig. 8.1).
- A high-pass filter (HPF) passes high frequencies.
- A band-pass filter (BPF) passes a band (range) of frequencies.
- A band-stop filter (BSF) passes high and low frequencies outside of a specified band.

The main characteristics of filters are amplitude-frequency - Fig. 8.2 and phase frequency - fig. 8.3. The amplitude-frequency response is the dependence of the filter transmission coefficient on frequency. The phasefrequency response is the dependence of the phase shift of the output signal relative to the input signal. The frequency of the frequency filter transmitter is expressed in decibels.

$$
\mathrm{K}[\mathrm{~dB}]=20 \lg \mathrm{~K},
$$

where: K [dB] - gain in decibels;
K is the gain in relative units:
K=Uout/Uin.


Figure 8.1 - Low pass filter (LPF)


Figure 8.2 - Graphic representation characteristic $\mathrm{K}=\mathrm{F}(\mathrm{f})$ in Bode Plotter


Figure 8.3 - Graphic representation characteristic $\varphi=F(f)$ in Bode Plotter
At the frequency $f_{0}$ of the equal signal, the maximum value $U_{\text {OUT }}$ decreases by $\sqrt{2}$ times. When $f>f_{0}$ the output voltage decreases with increasing frequency at a rate of $20 \mathrm{~dB} / \mathrm{dec}$, ie, with an increase in frequency 10 times (for a decade), $U_{\text {OUT }}$ decreases by 10 times. The frequency range from 0 to the $f_{0}$ LPF bandwidth is called.

High-frequency filters (HFF) are characterized by the same parameters as the LPF.

The main parameter for a band-stop filter (BSF) is the quasiresonance frequency $f_{0}$ :

$$
f_{0}=1 / 2 \pi R_{1} C_{1}
$$

The bandwidth of the T-bridge $\Delta f$ is defined as the frequency difference at which the output voltage $U_{\text {OUT }}$ of the filter (at a given $U_{I N}$ ) is 0.707 from the maximum value on the LPF and HPF slopes. Knowing $\Delta f$, you can determine the Q factor of the filter as:

$$
Q=f_{0} / \Delta f
$$

The calculation of the parameters of the scheme for the band-pass filter (BPF) is the same as for the BSF.

## Motion of work

Experiment №1
LPF research

1. Draw a pattern of fig. 8.4.
2. Connect the Body Plotter.
3. Determine the frequency response and phase response.
4. Determine the frequency $f_{0}$ response and compare with the estimated data.

5 Determine the offset angle for $f_{0}$.
6. Determine the rate of change in the transfer coefficient of the filter.


Figure 8.4 - Low pass filter
Experiment №2
A multi-line RC low pass filters research:
7. Draw a pattern of fig. 8.5.
8. Connect the Body Plotter.
9. Determine the frequency response.
10. Determine $f_{0}$ on the frequency response and compare with the estimated data.
11. Determine the offset angle for $f_{0}$.
12. Determine the rate of change in the transfer coefficient of the filter.

Experiment №3
High-frequency filter research
13. Draw a diagram of fig. 8.6.
14. Connect the Body Plotter.
15. Determine the frequency response.
16. Determine $f_{0}$ on the frequency response and compare with the estimated data.


Figure 8.5 - Two-point low-pass filter
17. Determine the offset angle for the $f_{0}$.
18. Determine the rate of change in the transfer coefficient of the filter.


Figure 8.6 - High pass filter
Experiment №4
A multi-line RC high frequency filters research:
19. Draw a pattern of fig. 8.7.
20. Connect the Body Plotter.
21. Determine the frequency response.
22. Determine $f_{0}$ on the frequency response and compare with the estimated data.
23. Determine the offset angle for $f_{0}$.
24. Determine the rate of change in the transfer coefficient of the filter.


Figure 8.7 - Three-Way HPF.
Experiment №5 - A band-stop filters research:
25. Draw a pattern of Fig. 8.8 and connect the Bode Plotter.
26. Determinate the frequency response.
27. Determine the frequency $f_{0}$ and bandwidth of the barrier by frequency response and compare it with the estimated data.
28. Determine the offset angle for the $f_{0}$.
29. Determine the quality factor of the filter

Experiment №6 - A band-pass filters research:
27. Draw a pattern of fig. 8.9 and connect the Bode Plotter.
28. Determinate the frequency response.
29. Determine the frequency $f_{0}$ and bandwidth of the barrier by frequency response and compare it with the estimated data.
30. Determine the offset angle for the $f_{0}$.
31. Determine the quality factor of the filter.


Figure 8.8 - Scheme of double T-shaped bridge


Figure 8.9 - Scheme of the Vina Bridge

## Control questions

1. What is a filter.
2. What are the main types of filters you know.
3. What is an amplitude-frequency characteristics and what parameters do they depend on.
4. What are the main parameters of the LPF you know.
5. What is decibel and decade.
6. Describe the principle of the band-pass filter and band-stop filter ( and what parameters they are characterized.
7. Where are the filters used?

## Laboratory work 9. The digital combination units.

Objective: the structure and operating principle of digital combination units.

Brief theoretical data: A logical node is a device that processes information digitally. Logical nodes are subdivided into combinational and memory nodes. The main property of combinational nodes - the input vector X uniquely determines the output Y . The main difference between the combinational nodes and the memory nodes is that the outputs in the memory nodes depend on the state (the previous work cycle). Typical logical nodes: decoder, multiplexer, binary adder, code converter.

Decoder is a logical device that converts the binary code of the number entered to the input into a signal on one of its outputs. The decoder is designed to convert the code information records into counters and registers into control signals and to transmit them to the control system's operating elements in the display device. The decoder scheme (fig.9.1) has several inputs and outputs. On the inputs A, B, C of the decoder comes the binary code of the number. For each code number the signal corresponds to one of 8 decoder outputs.


Figure 9.1 - Decoder
Inputs: G', A, B, C. Outputs: $0^{\prime}-7^{\prime}$.

## Motion of work

Experiment №1. - Reception of the decoder truth table.
1 Build the decoder schema shown in fig. 9.2.


Figure 9.2 - Diagram of connecting the decoder " 3 to 8 "
2. Fill the table of truth of the device (tabl. 9.1) - only 16 states, observing the outputs of the decoder in various combinations of its inputs. Operations are performed by changing the states using the 0 to 3 switches.

Table 9.1 - Dependence of decoder outputs from inputs

| $\mathrm{G}^{\prime}$ | C |  | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 |  | 0 | 0 |  |  |  |  |  |  |  |  |
| $\ldots$ | $\ldots$ |  | $\ldots$ | $\ldots$ |  |  |  |  |  |  |  |  |
| 1 | 1 |  | 1 | 1 |  |  |  |  |  |  |  |  |

Experiment 2 - Realization of arbitrary logic function by means of a decoder
3. Draw the schema shown in fig. 9.3, which implements the function $\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{C}$ ' $+\mathrm{AB}+\mathrm{BC}$


Figure 9.3 - Realization of a given logic function using a decoder
4. Program the word generator as shown in fig. 9.4


Figure 9.4 - Programming the word generator
5. Fill in the tabl. 9.2 for all combinations of input values, to do this, run the schema to run and press the "step" button in the word generator, to fix the states at the output of the circuit.
6. Using the "Logic converter" specify the truth of the table in paragraph 5 as shown in fig. 9.5

Table 9.2 - Truth Table for all combinations of input quantities

| $\mathrm{G}^{\prime}$ | C | B | A | Output |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 |  |
| $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ |  |
| 1 | 1 | 1 | 1 |  |



Figure 9.5 - Specifying the truth table in the "Logic converter"
7. Convert the truth table to the formula implemented by the decoder (button $101 \operatorname{simp} \rightarrow \mathrm{~A} \mid \mathrm{B}$ ). Compare the result with the original formula

Experiment 3 -Realization of arbitrary logic function
8. Develop a scheme that implements the logical function proposed by the instructor
9. Test the developed scheme according to the method described in experiment 2.

## Control questions

1 Determination of the combinational node, its difference from the node with memory.

2 Types of combinational units.
3 Principle of operation of the decoder and multiplexer.
4 Realization of arbitrary logic function by means of decoder.
5 Areas of use decoder, multiplexer.

## Laboratory work 10. Digital nodes with memory

Objective: to study the structure and principle of operation of RS, JK - triggers, counters; learn to design counters with a given conversion factor.

Brief theoretical data: in order to turn the combinational node into a memory node, use feedback. The memory node is characterized by two characteristic equations:
a) the outputs function

$$
\mathrm{Y}=\mathrm{f}(\mathrm{X}, \mathrm{~S})
$$

де Y - output signal; X - input signal; S - state.
б) the transition function

$$
S^{t+1}=f\left(S^{t}, X\right)
$$

where $\mathrm{S}^{\mathrm{t}}$ - state at the current time, $\mathrm{S}^{\mathrm{t}+1}$ - state at the next time.
Typical nodes with memory: trigger, counter, and register.
A trigger is an elementary memory node that can be in one of the two states of " 0 " or " 1 " and has two outputs of straight and inverse. By the functions, the triggers are divided into RS - triggers, D - triggers, T triggers, JK triggers and others.

RS-trigger has two installation inputs: S (set) and R (reset) settings, which are fed by incoming signals from external sources. When applying to the input of the installation of the active level of the logical signal, the trigger is set to " 1 ", and when the active level of the logical signal is applied to the input, the reset trigger is set to " 0 ". If at both inputs of the trigger passive logic levels of the input signal, then the trigger will save the previous state of the outputs. Each of these states is stable and is supported by feedback actions.

The JK-type trigger has a more complex, compared to the RS-trigger, internal structure, and wider functionality. In addition to the J and K information inputs, and the direct and inverse outputs, the JK trigger has a C control (actuation) control input, as well as an input terminal R and S . Constituent inputs have priority over all others. The active signal level at the input S sets the JK trigger to the state $\mathrm{Q}=1$, and the active level of the signal at the input R - to the state $\mathrm{Q}=0$, regardless of signals from other inputs. If the input voltages are at the same time applied to the passive
signal level, the trigger state will change at pulse recession at the input input, depending on the input state J and K .

A counter is a digital memory node built on triggers, which can be in one of the 2 n states, where n is the number of triggers. The digit count n is equal to the number of T triggers. Each input pulse changes the state of the counter, which persists until the next signal is received. The counter is one of the main functional nodes of the computer, as well as various digital controllers and information-measuring systems.

Characteristics:
a) information capacity is determined by the number of states in which the meter may be;
b) speed - maximum frequency of passage of pulses on the counter input.

Registers are triggers and data storage nodes.

## Motion of work

Experiment 1 - research RS - trigger

1. Draw a diagram depicted in fig. 10.1 (file 14_02 in the examples)
2. When changing the state at the inputs $S, R$, use the " $S$ " and "R" switches to fill in the tabl. 10.1

Experiment 2 - study JK - trigger
3. Make the JK scheme - a flip-flop, depicted in fig. 10.2 (file 14_03 in the examples)
4. Fill in the table 10.2. Set the JK trigger to its original state by specifying the sequence of incoming sets according to Table 10.2.
5. Fill in table 2.3 by specifying the sequence of input kits using the "J", "K", "C"

Experiment 3 - study of the counter
6. Draw the schema shown in fig. 10.3 (file $14 \_06$ in the examples).
7. Use the C switch to change the status of the counters. Enter the current states in tabl. 10.4.
$1 \mathrm{kOhm} / 5 \mathrm{~V}$


Figure 10.1 - Study scheme of RS-trigger
Table 10.1 - Transaction table

| R | S | Q | $\mathrm{Q}^{\prime}$ | Mode |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 1 |  |  |  |
| 1 | 1 |  |  |  |
| 1 | 0 |  |  |  |
| 1 | 1 |  |  |  |
| 0 | 0 |  |  |  |

Table 10.2 - Asynchronous table of JK-flip-flop transitions

| S | R | Q | $\mathrm{Q}^{\prime}$ |
| :---: | :---: | :---: | :---: |
| 0 | 1 |  |  |
| 0 | 0 |  |  |

Experiment 4 - study of a counter with a variable conversion factor
8. Draw the schema shown in fig. 10.4 (file 14_08.ca4 in the examples)
9. Fill in the tabl. 10.5

## $1 \mathrm{k} \mathrm{Ohm} / 5 \mathrm{~V}$



Figure 10.2 - Study scheme of the JK-trigger
Table 10.3 - Input kits, states and operating modes of the JK-trigger

| S | R | J | K | C | Q | Mode |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 0 | 0 |  |  |
| 0 | 0 | 0 | 0 | 1 |  |  |
| 0 | 0 | 0 | 0 | 0 |  |  |
| 0 | 0 | 1 | 0 | 0 |  |  |
| 0 | 0 | 1 | 0 | 1 |  |  |
| 0 | 0 | 1 | 0 | 0 |  |  |
| 0 | 0 | 0 | 1 | 0 |  |  |
| 0 | 0 | 0 | 1 | 1 |  |  |
| 0 | 0 | 0 | 1 | 0 |  |  |
| 0 | 0 | 1 | 1 | 0 |  |  |
| 0 | 0 | 1 | 1 | 1 |  |  |
| 0 | 0 | 1 | 0 | 0 |  |  |
|  |  |  |  |  |  |  |



Figure 10.3 - Scheme of research of three-bit binary counter
Experiment 5 - synthesis of a counter with a given coefficient of recalculation type (aggravated, subtracting)
10. Upgrade the circuit (fig. 10.4) in accordance with the individual task of the meter parameters
11. Check experimentally the table of states of the counter Table 10.4 - Table of counter states

| The state of the <br> upper BCD / DPY | The state of the lower <br> BCD / DPY | The state of the <br> triggers <br> Q3 Q2 Q1 |
| :---: | :---: | :---: |
|  |  |  |
|  |  |  |

Table 10.5-Table of states of the counter

| Input pulse <br> number | State counter <br> by indicator | The state of the <br> triggers <br> Q3 Q2 Q1 |
| :---: | :---: | :---: |
| 0 |  |  |
| 1 |  |  |
| 2 |  |  |
| 3 |  |  |
| 4 |  |  |
| 5 |  |  |



Figure 10.4 - A counter with a variable conversion factor

## Control questions

1. Determination of nodes with memory.
2. Typical memory nodes.
3. Classification of flip-flops, characteristics of counters, principles of operation of flip-flops, counters, registers.
4. Construction of a counter with a given conversion factor

## Laboratory work 11. The compensating voltage regulator

Objective: to study the structure and principle of the compensating voltage regulator. Investigate the voltage limits of the stabilizer and its load characteristics

Brief theoretical data: a voltage regulator is a device that automatically maintains a constant voltage on the load. It is characterized by the following parameters:

- the coefficient of stabilization - the relation of the instability of the input voltage to the instability at its output:

$$
K_{c}=\frac{\frac{\Delta U_{в x}}{U_{\text {вх.ном }}}}{\frac{\Delta U_{\text {вих }}}{U_{\text {вих.ном }}}}
$$

where $\Delta U^{b x}, \Delta U{ }^{6 u x}$ - change the input and output voltages respectively; $U_{\text {вх.ном }}, U_{\text {вих.ном }}$ - nominal input and output voltage, respectively.

- internal (output) resistance - this is the ratio of change in the output voltage $\Delta U_{\text {sux }}$ to the change in load current $\Delta I_{\text {bux }}$, which caused the change in voltage:

$$
r_{i}=\frac{\Delta U_{s u x}}{\Delta I_{\text {sux }}}
$$

- temperature coefficient voltage (TCV) - the ratio of voltage $\Delta U^{\text {sux }}$ change to the change in ambient temperature $\Delta t$ that caused the change in voltage:

$$
T C V=\gamma=\frac{\Delta U_{\Delta t x}}{\Delta t}
$$

In principle, the stabilizers are divided into compensatory and parametric ones. The principle of operation of parametric stabilizers is based on the use of devices that have non-linear volt-ampere characteristics. Silicon stabilizers are used to build such stabilizers. Compensation stabilizers work as a closed-loop automatic feedback control system.

## Motion of work

Experiment 1 - Research of the minimum allowable input voltage. 1 Collect the diagram shown in fig. 11.1 (Regulate in the Samples folder)

2 Increase voltage source V7 (see fig. 11.1)
3 Observe the input and output voltage form on the oscilloscope
4. Repeat items 2, 3 until the distortion of the output voltage form appears. Record the limit value of the input voltage.

Experiment 2 - Research of the maximum allowable input voltage
5. Update the initial value of $\mathrm{V} 7=0.707 \mathrm{~V}$
6. Increase the voltage of the V8 source (see fig. 11.1).
7. Observe the input and output voltage form on the oscilloscope
8. Repeat items 6,7 until the shape of the output voltage is distorted.
9. Record the limit value of the input voltage.

Experiment 3 - Study of the load characteristics of the stabilizer
9. Update the initial values of V7, V8.
10. Change the R25 and fix the Uout. Results are listed in tabl. 11.1.
11. Repeat item10 until the Uout decreases by $10 \%$ from the Uout nom $=13.5 \mathrm{~V}$.

12 Fix the resistance at which Uout $=13.5 \mathrm{~V}$ as the maximum permissible resistance.

Table 11.1 - Results of measurements

| $\mathrm{U}_{\text {out }}, \mathrm{B}$ |  |  |  |  |  |  |  |
| :---: | :---: | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{R}_{25}, \mathrm{Om}$ |  |  |  |  |  |  |  |
| $\mathrm{I}_{\text {out }}, \mathrm{A}$ |  |  |  |  |  |  |  |

13. Build a graph of the dependence of Uout and Iout and determine the limits of permissible resistance.


Figure 11.1 - Principle diagram of the compensating stabilizer

Legend: Q17, Q16, R21, R20 - comparison scheme; D11, R24 reference voltage source; V7, V8 - creates an input chain model; Q18, Q19 - an element regulated on a composite transistor; Q14, R17, R23, D10 current sources; R18, R19 - voltage dividers; R22, Q15, D9 - amplifier; R25-load.

## Control questions

1. The principle of the parametric stabilizer.
2. Principle of action of compensating stabilizer.
3. Block diagram of parametric and compensating stabilizers.
4. Concept of a serial and parallel compensating stabilizer.
5. Assignment of elements of the scheme under study.

## Laboratory work 12. The structure and operation of the DAC and ADC.

Objective: to study the structure and operation of the DAC and ADC.

Brief theoretical data: the main task of the ADC is the development of binary signal codes - a periodic sampling of the analog signal. According to the principle of operation, all existing ADC types can be divided into 2 groups:

- ADC with charge capacitor;
- ADC with comparison of the input signal with discrete voltage levels.

The principle of the operation of the DAC is to convert the digital code to resistance or load, which is why the main devices of the DAC are decoder input code with control keys and the resistor circuit. A simple DAC can be built on the basis of an inverting adder.

## Motion of work

Experiment number 1 - DAC research on the basis of an inverting adder

1. Collect the diagram shown in fig 12.1.
2. Use the $0-3$ switches to set different binary codes at the DAC input and observe the output voltage of the DAC. Include the results in tabl. 12.1.


Figure 12.1 - DAC based on an inverting adder
Table 12.1 - DAC research based on an inverting adder

| 3 | 2 | 1 | 0 | $U_{\text {out }}$ |
| :--- | :--- | :--- | :--- | :--- |
|  |  |  |  |  |
|  |  |  |  |  |

3 Determine the number of graduations, the output voltage range, and the maximum conversion error

Experiment 2 - Research of DAC with resistive matrix R-2R
4. Collect the diagram shown in fig. 12.2.


Figure 4.2 - DAC with resistive matrix R-2R
5. Use the " $0-3$ " switches to set different binary codes at the DAC input and observe the output voltage of the DAC. Include the results in tabl. 12.2.
6. Determine the number of graduations, the range of the output voltage and the maximum error of the transformation.

Table 12.2 - Research DAC with resistive matrix R-2R

| 3 | 2 | 1 | 0 | $U_{\text {out }}$ |
| :--- | :--- | :--- | :--- | :--- |
|  |  |  |  |  |

Experiment 3 - DAC research based on the EWB library
7. Collect the schema shown in fig. 12.3.
8. The word generator is programmed into the cyclic mode of word sequence execution ( $0000,0001, \ldots 00 \mathrm{FE}, 00 \mathrm{FF}$ ) with a frequency of 1 kHz
9. Using the oscilloscope to observe the voltage dependence on the output of the DAC from time to time. The oscillogram is redrawn to the report.


Figure 12.3 - DAC based on the EWB library

1. Advantages and Disadvantages of DAC Based on Inverting Adder and Resistive Matrix R-2R.
2. Purpose and structure of ADC.
3. Principle of DAC operation.
4. What determines the error of the DAC, the range of output voltage, the number of graduations of the output voltage.

## Laboratory work 13. The unipolar power regulator

Objective: to study the structure and principle of the unipolar power regulator.

Brief theoretical data: The power regulator is designed to control the average power in the load. It consists of a power transformer, a power element and a control circuit. Power elements are performed on thyristors or opto-thyristors. The control circuit is based on digital or analog principles and controls the delay of activating power elements relative to the moment of the transition time through the zero voltage of the network.

In this paper, a digital control circuit is investigated, in which the control signal code is entered in the subtractive counter at the moment of the network voltage transition through zero. Under the action of clock pulses state of the meter decreases. The signal for the activation of the power elements is formed at the moment of the switch of the counter to " 0 ".

## Motion of work

Experiment 1 - Research of the synchronization node with the power supply

1. Collect the diagram shown in fig. 13.1.
2. Watch at the output of the node short pulses of synchronization at the moment of zero voltage transition. Using the potentiometer and changing the conversion factor of the pq 4-16 transformer, maximally reduce the width of the pulses of synchronization. Determine the width of the pulses.
3. The oscillograms of the voltage at the output of the transformer and the output of the synchronization node are redrawn into the report.


Figure 13 - Reseach of network synchronization node
Experiment 2 - Research of the control circuit of the digital power regulator
4. Add the previous diagram (fig. 13.1) to the elements of the controlled digital delay as shown in fig. 13.2.


Figure 13.2 - Digital control circuitry of the power regulator
5. To adjust the generator to the mode of formation of rectangular pulses with frequency:

$$
f=2 f_{c}\left(2^{m}-1\right)
$$

where $f \mathrm{c}$ is the frequency of the network voltage; m - the number of digits in the code $(\mathrm{m}=4)$.
6. Set the various control codes using the "A", "B", "C", "D" switches. Measure the time delay of the pulse on activating the power element (RCO output) relative to the pulse of synchronization (LOAD input). Put results in the table, build a dependency graph $T_{\text {delay }}=f$ (code).

## Control questions

1. Structural scheme of the control unit.
2. One is a bipolar controller.
3. Principles of network synchronization node operation.
4. Types of power elements.

## RECOMMENDED LITERATURE

1 Learn About Electronics - Home Page (learnabout-electronics.org) [Electronic resource] Access mode https://learnaboutelectronics.org/index.php (дата звернення: 23.12.2023).

2 BASIC ELECTRONICS Student Handbook Class - XI CENTRAL BOARD OF SECONDARY EDUCATION Shiksha Kendra, 2, Community Centre, Preet Vihar, Delhi [Electronic resource] Access mode http://cbseacademic.nic.in/web material/Curriculum/Vocational/2018/Basi c_Electronics_XI.pdf (дата звернення: 23.12.2023).

3 Horn, Delton T. Basic electronics Theory $-4^{\text {th }}$ ed., TAB Books. Division of McGraw-Hill, New York. 692 p.

